

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

NOV 03 2003  
PATENT & TRADEMARK OFFICE

2823/P

Applicant: Mac Apodaca et al. § Group Art Unit: 2823  
Serial No.: 10/036,833 §  
Filed: December 31, 2001 §  
For: Adhesion Layer For A Polymer §  
Memory Device And Method §  
Therefor §  
Atty. Dkt. No.: ITO.0516US (P13085)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

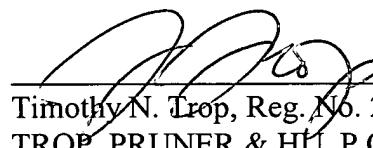
Dear Sir:

Applicant submits the references listed on the attached form PTO 1449 together with any required copies of such references.

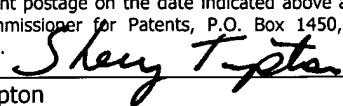
This statement is being filed after a first Office action on the merits, but before receipt of a final Office action or a Notice of Allowance. A check for \$180 in payment of the late submission fee of §1.17(p) is enclosed. Please apply any additional charges or credits to Deposit Account No. 20-1504 (ITO.0516US).

Respectfully submitted,

Date: 10/30/03

  
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10/04/2003 YPOLITE1 00000077 10036033  
01 FC:1806 180.00 0P

Date of Deposit: 10-31-03  
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.  
  
Sherry Tipton

<p style="text-align: center;"><b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)</p> <p style="text-align: center;">O I P 5 NOV 03 2003</p>				ATTY DOCKET NO. ITO.0516US (P13085)	SERIAL NO. 10/036,833	
				APPLICANT(S): MAC APODACA, JONG-WON S. LEE, KUO-WEI CHANG		
				FILING DATE: December 31, 2001	GROUP ART UNIT: 2823	
				<b>U.S. PATENT DOCUMENTS</b>		
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
A.						
B.						
C.						
D.						
<b>FOREIGN PATENT DOCUMENTS</b>						
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES      NO
E.						
F.						
G.						
H.						
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
I.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Jeong, U.I., Jeong, H.S. and Kim, Kinam, "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors," presented at 2003 19 <sup>th</sup> IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, California, February 26-20, 2003					
J.	Ha, Y.H., Yi, J.H., Horii, H., Park, J.H., Joo, S.H., Park, S.O., Chung, U-In and Moon, J.T., "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003					
K.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Oh, J.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Chung, U.I., Jeong, H.S. and Kim, Kinam, "Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24 mm-CMOS Technologies," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003					
L.	Horii, H., Yi, J.H., Park, J.H., Ha, Y.H., Baek, I.G., Park, S.O., Hwang, Y.N., Lee, S.H., Kim, Y.T., Lee, K.H., Chung, U-In and Moon, J.T., "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003					
M.						
N.						
O.						
EXAMINER			DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>						